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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,588	08/18/2003	Kitrick Sheets	1376.720US1	4010

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,588	SHEETS, KITRICK	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,9-11 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,9-11 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Request for Continued Examination (RCE) filed on September 25, 2006 regarding application 10,643,588 filed on August 18, 2003.

2. Claims 1, 4, 6, 9, 11 and 14 have been amended.

Claims 16-18 have been added.

Claims 2-3, 7-8 and 12-13 have been cancelled previously.

Claims 1, 4-6, 9-11 and 14-18 are pending under consideration.

3. ***Response to Remarks and Amendments***

Applicant's amendments and remarks have been fully and carefully considered. In response, a new ground of claim analysis based on a new reference (Vishin et al., US 5,860,146) has been made. Refer to the corresponding sections of the following claim analysis for details.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites "the method of claim 3, further comprising locating the ERTT header at a well known location to one or more nodes used by an application."

However, claim 3 has been cancelled previously. Thus claim 4 as currently presented depends from base claim that no longer exists.

Claim 5 is rejected by virtue of its dependence from claim 4.

In the subsequent claim analysis, the Examiner interprets claim 4 as "the method of claim 1, further comprising locating the ERTT header at a well known location to one or more nodes used by an application."

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4-6, 9-11 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Vichin et al. (US 5,860,146).

As to claim 1, Vichin et al. disclose **a method for translating a virtual memory address into a physical memory address** [Auxiliary Translation Lookaside Buffer for Assisting in Accessing Data in Remote Address Spaces (title); figure 5; The present invention relates generally to multiprocessor computer systems having virtual memory management subsystems, and particularly to a memory controller that manages access to remote physical addresses through the use of an auxiliary translation lookaside buffer (column 1, lines 5-10)] **in a multi-node system** [figure 1 shows a multi-node system where each cluster (102) represents a node connected together by a network (114)], **the method comprising**:

Initializing [in order for the remote translation mechanism disclosed by Vishin et al. to work and function properly, it is inherent that the RTT at all the nodes be initialized and synchronized first before any reference to a memory location resides at a remote node can be served. Without the initialization and synchronization, the RTT may not have the correct information to reach the correct memory location] **in a generally accessible memory** [figures 2 and 4 show that the RPTE comprising a DRAM (108)] **an emulated remote translation table (ERTT) segment** [figure 4 shows the Remote Page Table Entries (RPTE); figure 6];

providing the virtual memory address at a source node [The primary translation lookaside buffer translates a virtual address asserted by the data processor into a physical address. When the physical address does not correspond to a location in local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (column 3, lines 40-60)];

determining a virtual node to query based on the virtual memory address [figure 7, 170 shows the Node-ID field that provides the virtual node information];

accessing an ERTT header to obtain a mapping of the virtual node to a physical node [figure 7, 168 shows an ERTT header (the RPPA entry) comprising Node-ID, size, control flag and remote physical page address; figure 6 further shows that a plurality of the RPPA entries being organized and being accesses using the index V;

figure 5 illustrates how the mapping from a virtual node to a physical node is accomplished; The primary translation lookaside buffer translates a virtual address asserted by the data processor into a physical address. When the physical address does not correspond to a location in local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (column 3, lines 40-60)];

querying the ERTT segment on the physical node for the translation for the virtual memory address [figures 5-8 illustrates how this mapping is accomplished; The primary translation lookaside buffer translates a virtual address asserted by the data processor into a physical address. When the physical address does not correspond to a location in local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (column 3, lines 40-60)]; **and if the translation is received then loading the translation into a translation lookaside buffer (TLB) on the source node** [figures 5-8 illustrates how this mapping is accomplished; The primary translation lookaside buffer translates a virtual address asserted by the data processor into a physical address. When the physical address

does not correspond to a location in local memory, the RTLB determines whether the physical address matches at least one of the remote page table entries stored in the RTLB, and selects one of those remote page table entries when at least one match is found. Then, a remote physical address is generated by combining a portion of the selected remote page table entry with a portion of the physical address (column 3, lines 40-60)].

As to claim 4, Vishin et al. teaches **the method of claim 1, further comprising locating the ERTT header located at a well-known location to one or more nodes used by an application** [The computer system further includes a remote translation lookaside buffer (RTLB) that stores a plurality of remote page table entries. Each remote page table entry represents a mapping between a range of physical addresses and a corresponding range of remote physical addresses (abstract); figure 7, 168 shows an ERTT header (the RPPA entry) comprising Node-ID, size, control flag and remote physical page address; figure 6 further shows that a plurality of the RPPA entries being organized into a RTLB (Remote Translation Lookaside Table) and being accesses using the index V; figure 5 illustrates how the mapping from a virtual node to a physical node is accomplished; thus it is clear that an ERTT header can be located and obtained from the RTLB as shown in figure 6].

As to claim 5, Vishin et al. teaches that **the ERTT header is located on a predetermined virtual node** [The computer system further includes a remote translation lookaside buffer (RTLB) that stores a plurality of remote page table entries. Each remote page table entry represents a mapping between a range of physical

addresses and a corresponding range of remote physical addresses (abstract); figure 7, 168 shows an ERTT header (the RPPA entry) comprising Node-ID, size, control flag and remote physical page address; figure 6 further shows that a plurality of the RPPA entries being organized into a RTLB (Remote Translation Lookaside Table) and being accesses using the index V; figure 5 illustrates how the mapping from a virtual node to a physical node is accomplished; thus it is clear that an ERTT header can be located and obtained from the RTLB as shown in figure 6].

As to claim 6, refer to "As to claim 1" presented earlier in this Office Action. Further, Vishin et al. teaches that **an operating system executable by a source node of the plurality of nodes** [The 32 entries in the RTLB are organized into four groups of eight entries (entries 0:7, 8:15, 16:23 and 24:31). While the physical address ranges of the RPTEs in any one group may overlap, it is the responsibility of the operating system 180 (see FIG. 9) to make sure that the RPTEs in different groups do not have overlapping address ranges (column 5, lines 33-37)].

As to claim 9, refer to "As to claim 4" presented earlier in this Office Action.

As to claim 10, refer to "As to claim 5" presented earlier in this Office Action.

As to claim 11, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 14, refer to "As to claim 4" presented earlier in this Office Action.

As to claim 15, refer to "As to claim 5" presented earlier in this Office Action.

As to claim 16, Vishin et al. teaches **replicating the ERTT header on a plurality of nodes** [figure 1 shows a multi-node system where each cluster (102) represents a

node connected together by a network (114), and each cluster (102) has a copy of RTLB (160) of its own].

As to claim 17, refer to "As to claim 16" presented earlier in this Office Action.

As to claim 18, refer to "As to claim 16" presented earlier in this Office Action.

8. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Vishin et al. et al. (US 6,925,547), "Remote Address Translation in a Multiprocessor System."
- Scott, (US patent Application Publication 2004/0044872), "Remote Translation Mechanism for a Multi-Node System."
- Deneau, (US 6,684,305), "Multiprocessor System Implementing Virtual Memory Using a Shared Memory, and a Page Replacement Method for Maintaining Paged memory Coherence."
- Frank et al., (US 6,490,671), "System for Efficiently Maintaining Translation Lookaside Buffer Consistency in a Multi-Threaded, Multi-Processor Virtual Memory System."
- Hansen, (US 6,101,590), "Virtual Memory System with Local and Global Virtual Address Translation."

Conclusion

9. Claims 1, 4-6, 9-11 and 14-18 are rejected as explained above.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

October 19, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
11/06/06